

(19)



Europäisches Patentamt
European Patent Office
Office européen des brevets



(11)

EP 0 923 010 A2

(12)

EUROPEAN PATENT APPLICATION

(43) Date of publication:
16.06.1999 Bulletin 1999/24

(51) Int. Cl.⁶: **G05B 19/042**

(21) Application number: **98122521.2**

(22) Date of filing: **30.11.1998**

(84) Designated Contracting States:
**AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU
MC NL PT SE**
Designated Extension States:
AL LT LV MK RO SI

• Sunaga, Tsutomu,
Hitachi Nishi-ryo Room 309,
Kitakanbara-gun, Niigata 959-2604, (JP)
• Seki, Kenji
Toyosaka-shi, Niigata 950-3321 (JP)

(30) Priority: **12.12.1997 JP 34313897**

(71) Applicant: **Hitachi, Ltd.**
Chiyoda-ku, Tokyo 101 (JP)

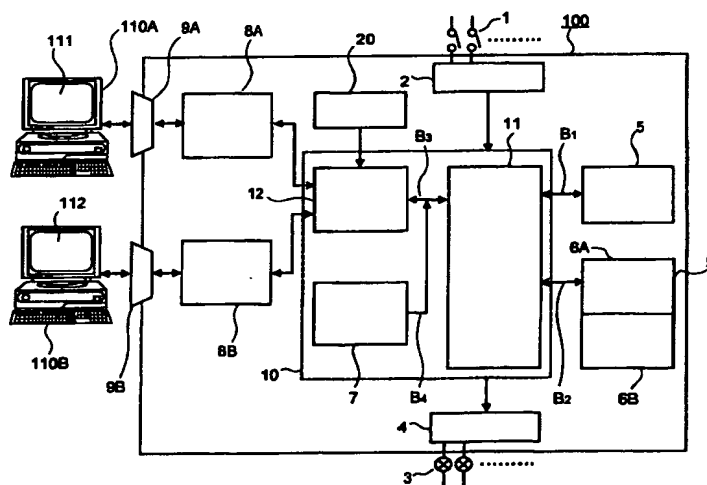
(72) Inventors:
• Kikuchi, Tadanori,
Kikuchi Apt. Room 16
Niigata 950-3116 (JP)

(74) Representative:
Altenburg, Udo, Dipl.-Phys. et al
Patent- und Rechtsanwälte
Bardehle - Pagenberg - Dost - Altenburg -
Geissler - Isenbruck,
Gallileiplatz 1
81679 München (DE)

(54) Programmable controller

(57) A programmable controller includes a first port 9A for communicating with a first peripheral apparatus 110A, a first interface portion 8A connected with the first port 9A, a second port 9B for communicating with a second peripheral apparatus 110B, a user program memory 6 for storing a user program, a main processor 11 for performing an operation according to the user program, and a sub processor 12 disposed so as to communicate with the first interface portion 8A, the second

interface portion 8B and said main processor 11. The user program memory 6 is divided into at least two memory areas 6A, 6B, and the sub processor 12 controls communication of the first port 9A and the second port 9B with the memory areas 6A, 6B. A programmable controller convenient and efficient in trouble shooting is obtained by this invention.

FIG.1

EP 0 923 010 A2

Description

BACKGROUND OF THE INVENTION

Technical Field of the Invention

[0001] This invention relates to a programmable controller including a plurality of processors for performing sequence operations, which has a port and an interface portion for communicating with a plurality of peripheral apparatus, and enables editing programs and monitoring performances simultaneously.

Description of Related art

[0002] A programmable controller 101 having two processors for performing sequence operations in the prior art is disclosed in Fig. 9.

[0003] As is disclosed, a central processing portion 10 includes a main processor 11, a sub processor 12 and a system program memory 7. The main processor 11 and the sub processor 12 are connected through a bus 20, and the system program memory (hereinafter system memory) 7 is connected with the bus B3 through a bus B4. Thus, either one of the main processor 11 and the sub processor 12 can access the system memory 7 through the bus B3 and B4. The main processor 11 is connected not only to a data memory 5 through a bus B1 but also to a user program memory (hereinafter user memory) 6 through a bus B2. A system program of the sub processor 12 is stored in the system memory 7, a user program is stored in the user memory 6 and I/O data such as results of operations are stored in the data memory 5. The sub processor 12 is connected to a port 9 through an interface portion 8 so as to communicate with a peripheral apparatus 110. Thus, the programmable controller 101 forms a programmable controller system together with input devices such as contacts, transducers or sensors 1 (not indicated in Fig. 9) and with output devices such as relays, contactors, solenoids or stepping motors 3 (not indicated in Fig. 9).

[0004] In this related art, the main processor 11 is designed to operate or handle basic commands of simple bit-operations such as ON-OFF commands for contacts or coils, while the sub processor 12 is designed to operate or handle complicated commands such as arithmetic commands or application commands other than the basic commands. The sub processor 12 also executes respondent operation for the peripheral apparatus 110 and internal operations for the commands from the peripheral apparatus 110. The peripheral apparatus 110 can communicate with the main processor 11 through the port 9 and the interface portion 8 to the user memory 6, which enables to store a ladder-program composed thereby in the user memory 6 and also enables monitoring an operation process.

[0005] Since the programmable controller in the related art is equipped with only a single set of the inter-

face portion 8 and the port 9 for communicating with the peripheral apparatus 110, a user is forced to alternate screens of a display 111 of the peripheral apparatus 110 from a monitoring screen to a program-editing screen, or vice versa. For instance, when the user adjusts a performance of the programmable controller system at its start, he or she must change the screen from that of monitoring to that of program-editing to edit or debug the user program, and he or she must change the screen reversely to the monitoring screen from the program-editing screen after confirmation of the performance is over. When the performance of the programmable controller system is not working as is conceived, this procedure i.e., alternating screens, is required repeatedly to find out a cause of an error, which brings about inconvenience and troublesomeness in the trouble shooting.

SUMMARY OF THE INVENTION

[0006] It is therefore an object of the present invention to solve the problems of the related art explained above. In view of the objective of solving the problems explained above, the programmable controller of the present invention includes an input port 2 for taking in an external signal, an output port 4 for outputting a signal for driving an external load, a first port 9A for communicating with a first peripheral apparatus 110A, a first interface portion 8A connected with said first port 9A, a user program memory 6 for storing a user program, a main processor 11 for performing an operation according to the user program, a data memory 5 for storing a result of the operation performed by the main processor 11, a sub processor 12 disposed so as to communicate with the first interface portion 8A and the main processor 11, and a system program memory 7 for storing a system program controlling the main processor 11 and the sub processor 12, wherein the main processor handles a basic command and said sub processor handles an application command, characterized in that the programmable controller further includes a second port 9B for communicating with a second peripheral apparatus 110B, the user program memory 6 is divided into at least two memory areas 6A, 6B, and the sub processor 12 controls communication of the first port 9A and the second port 9B with the memory areas 6A, 6B.

[0007] According to a preferred embodiment, the programmable controller further includes a second sub processor 12B. The first port 9A communicates with the memory areas 6A, 6B controlled by the sub processor 12 and the second port 9B communicates with the memory areas 6A, 6B controlled by the second sub processor 12B.

[0008] According to another embodiment, the programmable controller further includes a first peripheral apparatus 110A and a second peripheral apparatus 110B. The first peripheral apparatus is capable of monitoring a performance and editing the user program. The

first peripheral apparatus is capable of accessing to the memory areas 6A, 6B through the port 9A. The second peripheral apparatus is capable of monitoring a performance and editing the user program. The second peripheral apparatus is capable of accessing to the memory areas 6A, 6B through the port 9B.

[0009] A programmable controller convenient and efficient in trouble shooting is obtained by this invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The foregoing and a better understanding of the present invention will become apparent from the following detailed description of exemplary embodiments and the claims when read in connection with the accompanying drawings, all forming a part of the disclosure hereof this invention. While the foregoing and following written and illustrated disclosure focuses on disclosing exemplary embodiments of the invention, it should be clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and the scope of the present invention being limited only by the terms of the appended claims.

[0011] The following represents brief descriptions of the drawings, wherein:

Fig. 1 shows a block diagram of a programmable controller in one embodiment of the present invention.

Fig. 2 shows a chart explaining a flow of a process in a sub processor in one embodiment of the present invention.

Fig. 3 shows a block diagram of a main processor in one embodiment of the present invention.

Fig. 4 shows an example of a program stored in a user program memory in one embodiment of the present invention.

Fig. 5 shows a block diagram of a programmable controller in the second embodiment of the present invention.

Fig. 6 shows a block diagram of a programmable controller in the third embodiment of the present invention.

Fig. 7 shows a block diagram of a programmable controller in the fourth embodiment of the present invention.

Fig. 8 shows a block diagram of a programmable controller forming a basis for all embodiments of the present invention.

Fig. 9 shows a block diagram of a programmable controller in a related art.

DETAILED DESCRIPTION OF THE INVENTION

[0012] Before beginning a detailed description of the subject invention, mention of the following is in order. When appropriate, like reference numerals and characters are used to designate identical, corresponding or

similar components in differing figure drawings.

[0013] Exemplary embodiments of the present invention will now be explained with reference to Figs. 1 to 8. First, one embodiment of the present invention is explained referring to Figs. 1 through 4, and 8. Fig. 8 discloses a basic construction of a programmable controller (hereinafter PC) 100. The PC 100 generally includes a central processing portion 10, a system program memory (hereinafter system memory) 7, a user program memory (hereinafter user memory) 6, a data memory 5, an input port 2, an output port 4, an interface portion 8 and a port 9.

[0014] The central processing portion 10 not only handles operations such as logic operation or arithmetic operation but also controls another elements included in the PC 100. The system memory 7 is connected with the central processing portion 10 and stores a system program including contents and procedures of operation of the central processing portion 10. The user memory 6, which is a read/write memory capable of rewriting the program stored therein, is also connected with the central processing portion 10 and stores the user program. The data memory 5, which is a read/write memory capable of rewriting the program stored therein, is connected with the central processing portion 10 and stores the data such as operation results of the central processing portion 10. The input port 2 is connected with the central processing portion 10 and disposed so as to enable a connection with the input device 1 for transferring an input signal therefrom. The output port 4 is connected with the central processing portion 10 and disposed so as to enable a connection with the output device 3 for transferring an output signal thereto. The input device 1 includes elements such as contacts, transducers or sensors, and the output device 3 includes elements such as relays, contactors, solenoids or stepping motors. The port 9 is disposed so as to enable a connection with the peripheral apparatus 110, and is connected with the central processing portion 10 through the interface portion 8. Further, PC 100 of the present invention has at least one sub processor 12 and at least one additional set of a port 9 and an interface portion 8.

[0015] Fig. 1 shows a block diagram of PC of one embodiment of the present invention. PC 100 includes a sub processor 12, a set of a port 9B and an interface portion 8B and a switch 20 in addition to the basic construction. As shown in Fig. 1, the sub processor is disposed within the central processing portion 10 and is connected with the main processor 11 through a bus B3. The sub processor is also connected with the system memory 7 through the bus B3 and a bus B4 so as to be controlled by the system program. The data memory is connected with the central processing portion through a bus B1 and the user memory is connected with the central processing portion 10 through a bus B2. A combination of a port 9A and an interface portion 8A and a combination of the port 9B and the interface por-

tion 8B are connected with the sub processor 12, which enables the sub processor 12 to communicate with two peripheral apparatus 110A and 110B. In this embodiment, the peripheral apparatus 110A has a display screen 111 and is disposed so as to be connected with the port 9A. Similarly, the peripheral apparatus 110B has a display 112 and is disposed so as to be connected with the port 9B. The user memory is divided into a plurality of areas corresponding to the numbers of the sets of the port 9 and the interface portion 8, i.e., the numbers of the peripheral apparatus 110 to be connected. In this embodiment, the user memory is divided into two areas 6A, 6B for storing the user programs composed by the user using the peripheral apparatus 110A, 110B respectively. The switch 20 sets the numbers of the user programs to be executed, sets a destination of the user program within the user memory 6, i.e., 6A or 6B, and selects the user program to be executed by the sub processor 12 from those stored in the areas of the user memory 6A and 6B. Since the sub processor 12 controls communication of the first port 9A and the second port 9B with the memory areas 6A, 6B, the first peripheral apparatus 110A is capable of accessing to the memory areas 6A, 6B through the port 9A and the second peripheral apparatus 110B is capable of accessing to the memory areas 6A, 6B through the port 9B. Thus, each of the user program composed by the user using the peripheral apparatus 110A and the user program composed by the user using the peripheral apparatus 110B is taken into the sub processor 12 via interface portion 8A, 8B respectively, and is stored in either one of the areas of the user memory 6A, 6B according to the destination set by the switch 20. When the sub processor 12 performs a sequence operation, it executes selected one of the user programs stored in the user memory 6A, 6B according to the setting of the switch 20.

[0016] Fig. 2 shows a chart explaining a flow of a process in a sub processor in one embodiment of the present invention. As is shown in Fig. 2 (a), the sub processor executes a main program stored in the system memory 7. It also performs a direct memory access (hereinafter DMA) transfer from the peripheral apparatus 110A, 110B in parallel to the execution of the main program. When the sub processor performs the DMA transfer, data from the peripheral apparatus 110A, 110B are received at ports 9A, 9B respectively, and the sub processor 12 processes the data at ports 9A, 9B and stores contents of the process for the data 9A, 9B in different memory area respectively. At this time, the sub processor 12 performs an interrupt for the main program by a timer, and judges priority in the processes, and performs the process having the highest priority. As is shown in Fig. 2 (b), the sub processor judges a completion of receiving on a communication protocol. When at least either one of the ports 9A, 9B is receiving data from corresponding peripheral apparatus 110A, 110B, the sub processor 12 performs other jobs. When receiv-

ing of the data is completed, the sub processor 12 executes performance such as editing the program, monitoring, and I/O set according to a communication command as a process for ports.

[0017] A construction of the main processor 11 is shown in Fig. 3. The main processor 11 includes an address generator 30, a controller 31, a decoder 32, a program counter register 33, a program address register A 34 and a program address register B 35. The controller 31 is connected with the address generator 30 and the decoder 32 so as to be able to communicate with either of them. Both of the address generator 30 and the decoder 32 are connected with the sub processor 12 through a bus 40. The address generator 30 is connected with the data memory 5 through a bus 41 and also connected with the user memory 6 through a bus 42, a selector 48 and a bus 44. The decoder 32 is connected with the program counter 33, the program address register A 34 and the program address register B 35 through buses 46. The program counter 33, the program address register A 34 and the program address register B 35 are connected with the data memory 5 and the user memory 6 through a bus 45. The program counter 33 is also connected with the user memory 6 through a bus 43, the selector 48 and the bus 44. The controller 31 is connected with the user memory through a bus 47, the selector 48 and the bus 44. When the sub processor accesses the user program 6a or 6b, an address data is transferred to the address generator 30 within the main processor 11, where the address data is decoded and an address signal is generated and outputted on the bus 42. This address signal represents a rewritable space address within the user memory 6A and 6B. In this embodiment, the user memory 6A and 6B is constructed by dividing the memory 6 according to an address of the memory area. The user memory 6a, 6B can also be constructed by individual memory chips. The sub processor 12 can access either one of the user memory by changing the address. The address generator 30 also generates an address in the data memory 5 and outputs on the bus 41.

[0018] The memory area in the user memory 6A, 6B is divided by the address, and an information about this division is controlled by an address that represents the first position of the divided memory area (hereinafter head address). The sub processor 12 stores this head address within the the program address register A 34 and the program address register B 35 beforehand. The sub processor 12 refers to the head address in case of accessing the user program 6A, 6B by a request of the peripheral apparatus 110A, 110B. For instance, in case of referring to the Nth (N is a positive integer) step of the user program, the sub processor 12 accesses an address which is N ahead from the head address stored in the program address register A 34.

[0019] When the main processor 11 executes the user program, the sub processor 12 stores a head address of the user program to be executed in the program counter

register 33. When the main processor 11 is started, the main processor 11 executes the user program sequentially counting up the program counter register 33. The contents of the program counter register 33 is supplied to the main processor 11 as an address of the user memory 6A, 6B. The main processor can access the program counter register 33, the program address register A 34 and the program address register B 35, when they are selected by respective select signals 46a, 46b, 46c generated in the decoder 32 and outputted on the bus 46 in accordance with a signal outputted on bus 40 by the sub processor 12.

[0020] As shown in Fig. 4, the user memory 6A, 6B are divided into a plurality of areas (in this case, two areas). The first position of the divided memory area has its head address respectively, and the sub processor 12 controls the area defined from the head address, "m" or "n" to the last step including "END" as a user program. A plurality of user programs defined above are stored in the user memory 6.

[0021] As described above, the user memory 6 (6A, 6B) has a function of storing a plurality of user programs each including a head address, the sub processor 12 has a function of being capable of accessing either one of the divided areas of the user memory. The sub processor 12 also has a function of communicating with the peripheral apparatus 110A, 110B. In this invention, these functions are combined, which enables the peripheral apparatus 110A, 110B to access the divided areas 6A, 6B of the user memory 6 through the sub processor 12 respectively, and to display contents of the area 6A, 6B on their display screens 111, 112 respectively. Thus, the peripheral apparatus can perform different kind of processes or jobs at the same time. And the programmable controller in this embodiment can perform monitoring and editing of the program at the same time, when a plurality of peripheral apparatus each having a display screen are connected.

[0022] The second embodiment of the present invention is explained referring to Fig. 5.

[0023] In this embodiment, the PC 100 is also capable of connecting two peripheral apparatus 110A, 110B. PC 100 includes a sub processor 12 which is divided in two sub processors 12A, 12B, two sets of port and interface portion, i.e., a port 9A and an interface portion 8A and a port 9B and an interface portion 8B, a system memory 7 which is divided into two system memories 7A, 7B, a main processor 11, a bus controller 13, a switch 20, a data memory 5, a user memory divided into two areas 6A, 6B, an input port 2, and an output port 4. As shown in Fig. 5, the sub processors 12A, 12B are disposed within the central processing portion 10 and are connected with the main processor 11 through the bus controller 13. The bus controller 13 controls and switches the bus in such a manner that the sub processors can read the program to be processed when the sub processors 12A, 12B access the user memories 6A, 6B respectively or when the sub processors 12A, 12B

accesses the data memory 5. The sub processor 7A is connected with the system memory 7A and the sub processor 7B is connected with the system memory 7B so as to be controlled by the system program. The system memory 7A stores a first system program and the system memory 7B stores a second system program. The first system program is not necessarily the same to the second system program. The sub processors 12A, 12B are connected with the main processor 11 through the bus controller 13. The data memory 5 is connected with the central processing portion 10 through a bus and the user memory 6 is connected with the central processing portion 10 through a bus. The combination of the port 9A, the interface portion 8A and the sub processor 12A enables the sub processor 12A to communicate with the peripheral apparatus 110A. The combination of the port 9B, the interface portion 8B and the sub processor 12B enables the sub processor 12B to communicate with the peripheral apparatus 110B. The peripheral apparatus 110A, 110B have the display screens 111, 112 respectively. The user memory 6 is divided into two areas 6A, 6B for storing the user programs composed by the user using the peripheral apparatus 110A, 110B respectively. The switch 20 is connected with the bus controller 13 and sets the numbers of the user programs to be executed, sets a destination of the user program within the user memory 6, i.e., 6A or 6B, and selects the user program to be executed by the sub processor 12 from those stored in the areas of the user memory 6A and 6B. An information of many kinds of setting for the user memory 6A, 6B by the switch 20 is stored in a register (not shown in Fig. 5) in the bus controller 13, which enables the sub processors 12A, 12B to read the information of the switch 20 by accessing the register. Thus, each of the user program composed by the user using the peripheral apparatus 110A and the user program composed by the user using the peripheral apparatus 110B is taken into the sub processor 12A, 12B via interface portion 8A, 8B respectively, and is stored in either one of the areas of the user memory 6A, 6B according to the destination set by the switch 20. When the sub processor 12 performs a sequence operation, it executes selected one of the user programs stored in the user memory 6A, 6B according to the setting of the switch 20. In this embodiment, efficiency of monitoring and editing is improved.

[0024] The third embodiment of the present invention is explained referring to Fig. 6.

[0025] In this embodiment, the PC 100 is also capable of connecting two peripheral apparatus 110A, 110B. PC 100 includes a sub processor 12 which is divided in two sub processors 12A, 12B, two sets of port and interface portion, i.e., a port 9A and an interface portion 8A and a port 9B and an interface portion 8B, a system memory 7 which is divided into two system memories 7A, 7B, a main processor 11, a switch 20, a data memory 5, a user memory divided into two areas 6A, 6B, an input port 2, and an output port 4. As shown in Fig. 6, the sub

processors 12A, 12B are disposed within the central processing portion 10 and are connected with the main processor 11. The sub processor 7A is connected with the system memory 7A and the sub processor 7B is connected with the system memory 7B so as to be controlled by the system program. The system memory 7A stores a first system program and the system memory 7B stores a second system program. The first system program is not necessarily the same to the second system program. The sub processors 12A, 12B are connected with the main processor 11. The data memory 5 is connected with the central processing portion 10 through a bus and the user memory 6 is connected with the central processing portion 10 through a bus. The combination of the port 9A, the interface portion 8A and the sub processor 12A enables the sub processor 12A to communicate with the peripheral apparatus 110A. The combination of the port 9B the interface portion 8B and the sub processor 12B enables the sub processor 12B to communicate with the peripheral apparatus 110B. The peripheral apparatus 110A, 110B have the display screens 111, 112 respectively. The user memory 6 is divided into two areas 6A, 6B for storing the user programs composed by the user using the peripheral apparatus 110A, 110B respectively. The switch 20 is connected with the main processor 11 and sets the numbers of the user programs to be executed, sets a destination of the user program within the user memory 6, i.e., 6A or 6B, and selects the user program to be executed by the sub processor 12 from those stored in the areas of the user memory 6A and 6B. All information of many kinds of setting for the user memory 6A, 6B by the switch 20 is stored in a register (not shown in Fig.6) in the main processor 11, which enables the sub processors 12A, 12B to read the information of the switch 20 by accessing the register. Thus, each of the user program composed by the user using the peripheral apparatus 110A and the user program composed by the user using the peripheral apparatus 110B is taken into the sub processor 12A, 12B via interface portion 8A, 8B respectively, and is stored in either one of the areas of the user memory 6A, 6B according to the destination set by the switch 20. When the sub processor 12 performs a sequence operation, it executes selected one of the user programs stored in the user memory 6A, 6B according to the setting of the switch 20. In this embodiment, efficiency of monitoring and editing is improved. Further this embodiment can simplify its construction because no bus controller 13 is employed when compared to the second embodiment.

[0026] The fourth embodiment of the present invention is explained referring to Fig. 7.

[0027] In this embodiment, the PC 100 is capable of connecting three peripheral apparatus 110A, 110B, 110C. The peripheral apparatus 110C has a display screens 113 similarly to the peripheral apparatus 110A, 110B. In order to connect three peripheral apparatus, PC 100 includes an extra set of a port 9C and an inter-

face portion 8C in addition to the two sets of port and interface portion, i.e., the port 9A and the interface portion 8A and the port 9B and the interface portion 8B, disclosed in Fig.6. In this embodiment, the sub processor 12B communicates with two peripheral apparatus 110B, 110C, through the port 9B and the interface portion 8B and the port 9C and the interface portion 8C respectively. The user memory 6 is divided into three areas 6A, 6B, 6C for storing the user programs composed by the user using the peripheral apparatus 110A, 110B, 110C respectively. The switch 20 is connected with the main processor 11 and sets the numbers of the user programs to be executed, sets a destination of the user program within the user memory 6, i.e., 6A, 6B or 6C, and selects the user program to be executed by the sub processor 12 from those stored in the areas of the user memory 6A, 6B and 6C. An information of many kinds of setting for the user memory 6A, 6B, 6C by the switch 20 is stored in a register (not shown in Fig. 7) in the main processor 11, which enables the sub processors 12A, 12B, to read the information of the switch 20 by accessing the register. Thus, the user program composed by the user using the peripheral apparatus 110A is taken into the sub processor 12A via interface portion 8A and the user programs composed by the user using the peripheral apparatus 110B, 110C are taken into the sub processor 12B via interface portion 8B. Each of these programs is stored in either one of the areas of the user memory 6A, 6B, 6C according to the destination set by the switch 20. The other construction is the same as the third embodiment.

[0028] As described above, above embodiments can perform monitoring and program-editing simultaneously, which provides a programmable controller having high efficiency.

[0029] This concludes the description of the preferred embodiments. Although the present invention has been described with reference to a number of illustrative embodiments thereof it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this invention. More particularly, reasonable variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the foregoing disclosure, the drawings and the appended claims without departing from the spirit of the invention. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

Claims

1. A programmable controller including an input port 2 for taking in an external signal, an output port 4 for outputting a signal for driving an external load, a first port 9A for communicating with a first peripheral apparatus 110A, a first interface portion 8A

connected with said first port 9A, a user program memory 6 for storing a user program, a main processor 11 for performing an operation according to said user program, a data memory 5 for storing a result of said operation performed by said main processor 11, a sub processor 12 disposed so as to communicate with said first interface portion 8A and said main processor 11, and a system program memory 7 for storing a system program controlling said main processor 11 and said sub processor 12, wherein said main processor handles a basic command and said sub processor handles an application command, characterized in that said programmable controller further includes a second port 9B for communicating with a second peripheral apparatus 110B, a second interface portion 8B connected with said second port 9B, said user program memory 6 is divided into at least two memory areas 6A, 6B, and said sub processor 12 controls communication of said first port 9A and said second port 9B with said memory areas 6A, 6B.

2. A programmable controller according to claim 1, further including a second sub processor 12B, wherein said first port 9A communicates with said memory areas 6A, 6B controlled by said sub processor 12 and said second port 9B communicates with said memory areas 6A, 6B controlled by said second sub processor 12B.
3. A programmable controller according to claim 1, further including a first peripheral apparatus 110A and a second peripheral apparatus 110B, wherein said first peripheral apparatus is capable of monitoring a performance and editing said user program, said first peripheral apparatus is capable of accessing to said memory areas 6A, 6B through said port 9A, said second peripheral apparatus is capable of monitoring a performance and editing said user program, and said second peripheral apparatus is capable of accessing to said memory areas 6A, 6B through said port 9B.

45

50

55

FIG. 1

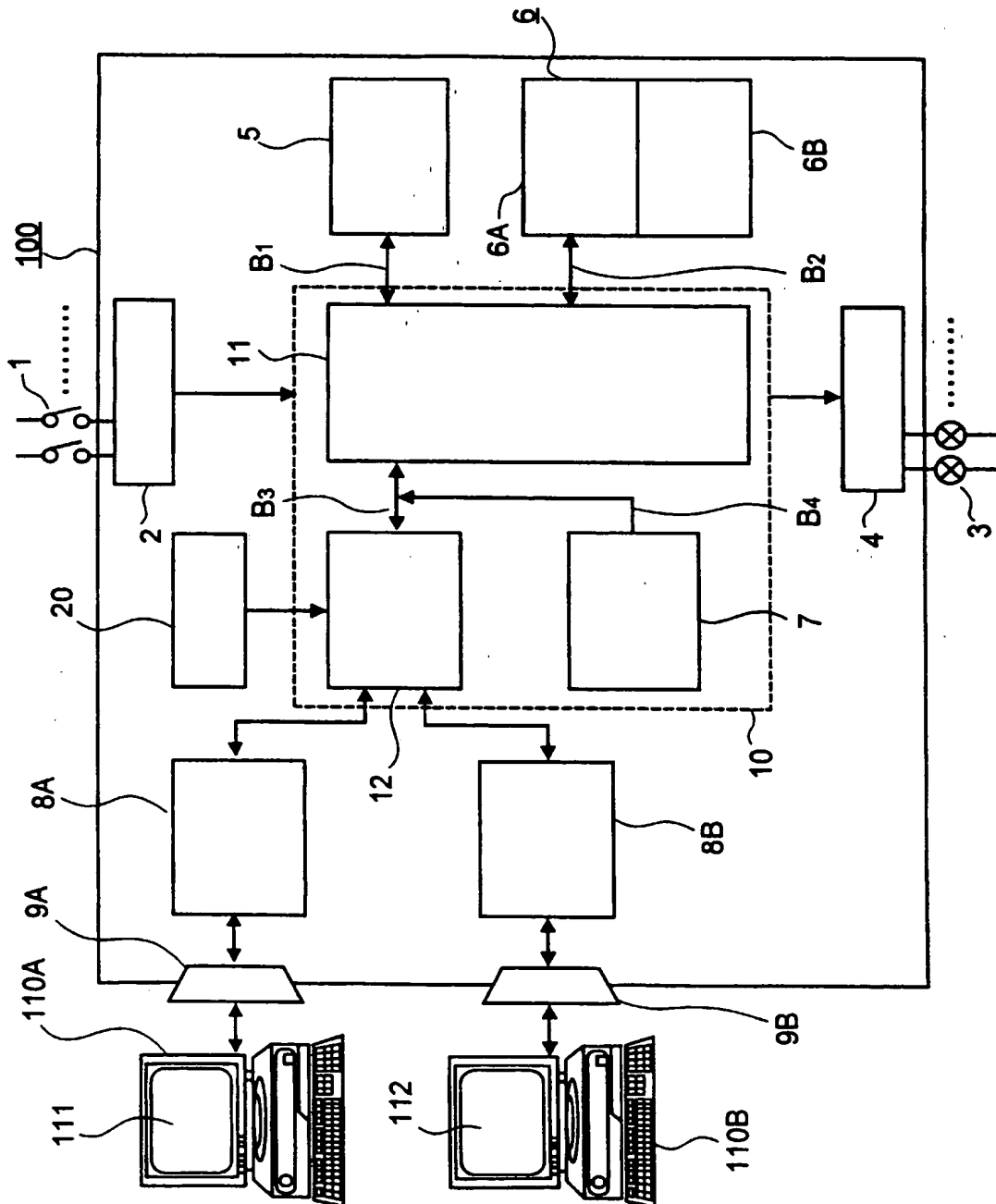


FIG.2

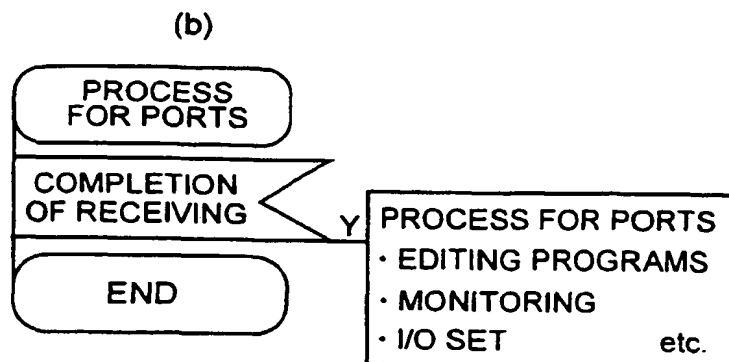
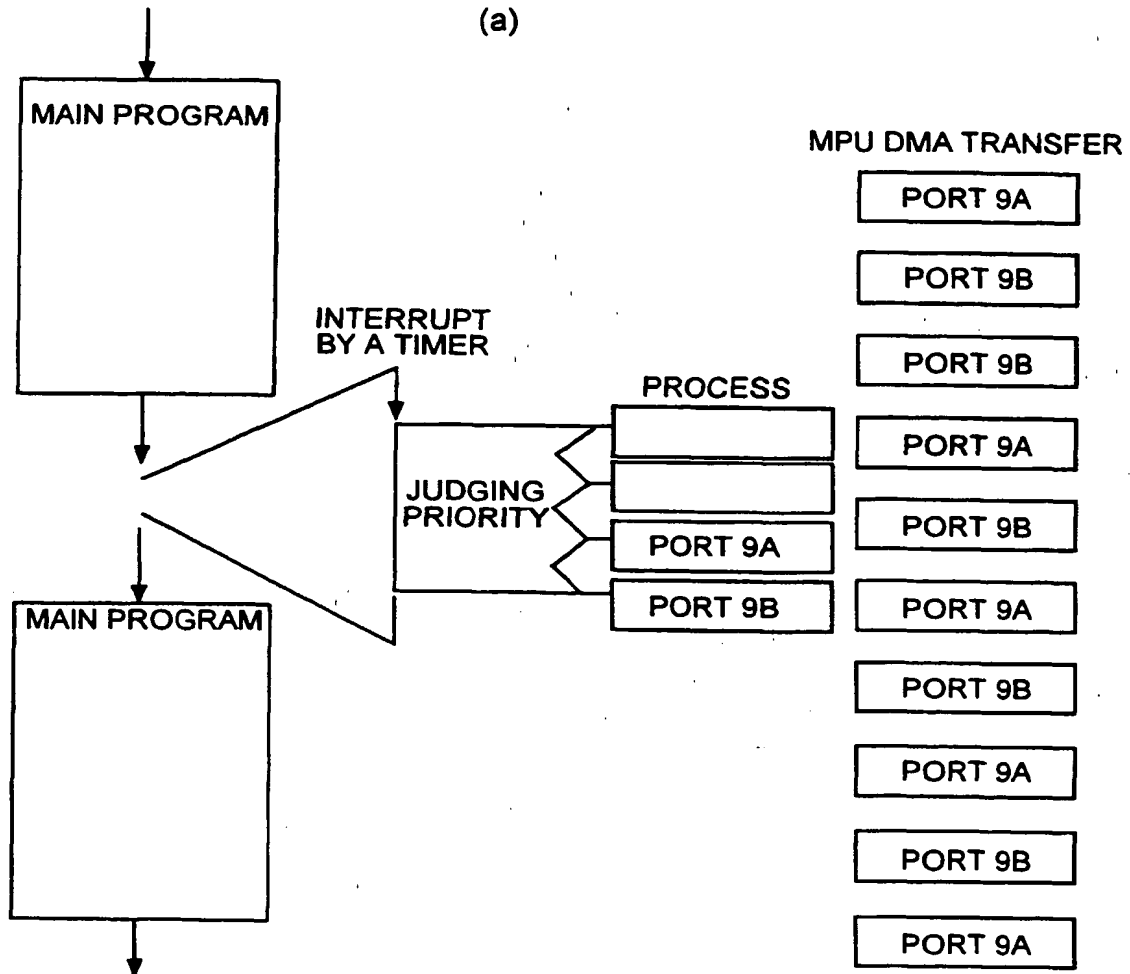


FIG.3

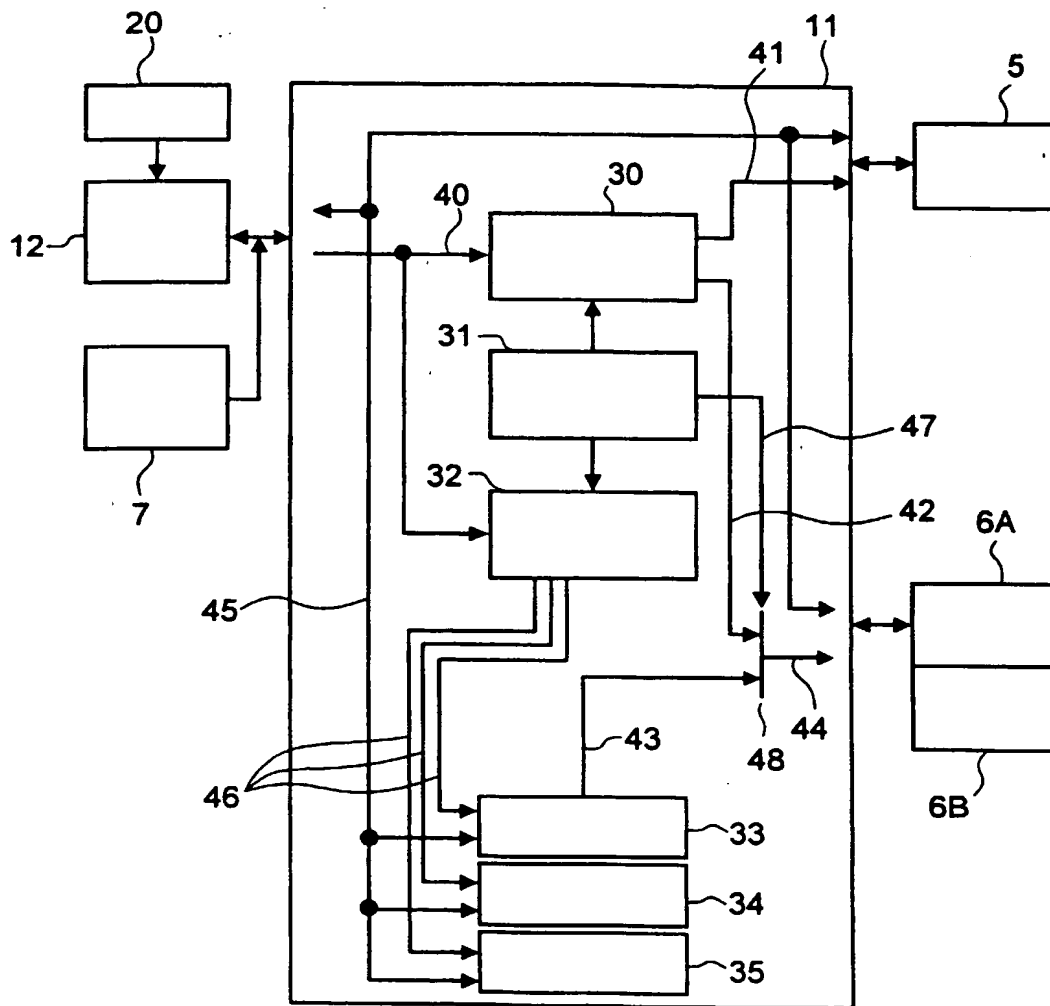


FIG.4

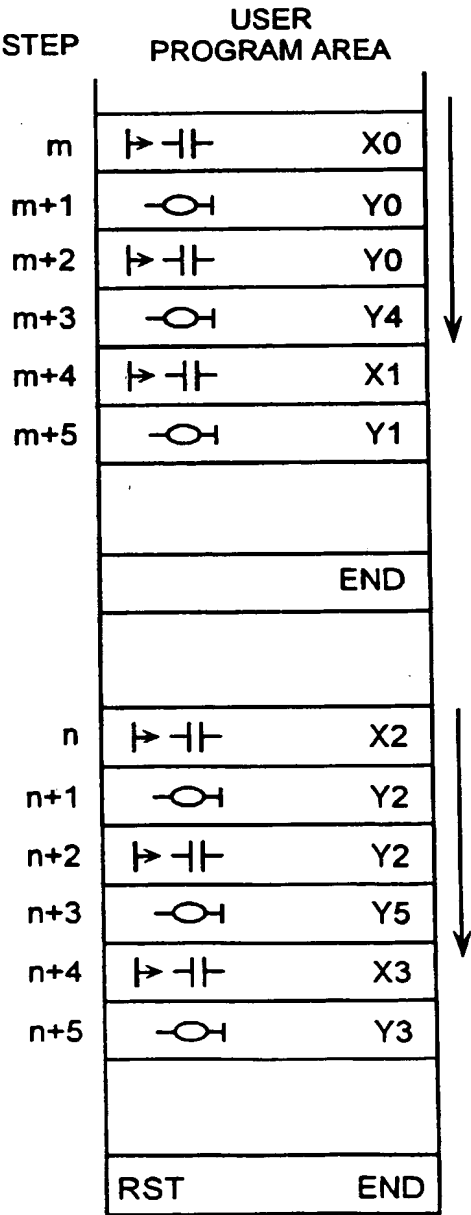


FIG.5

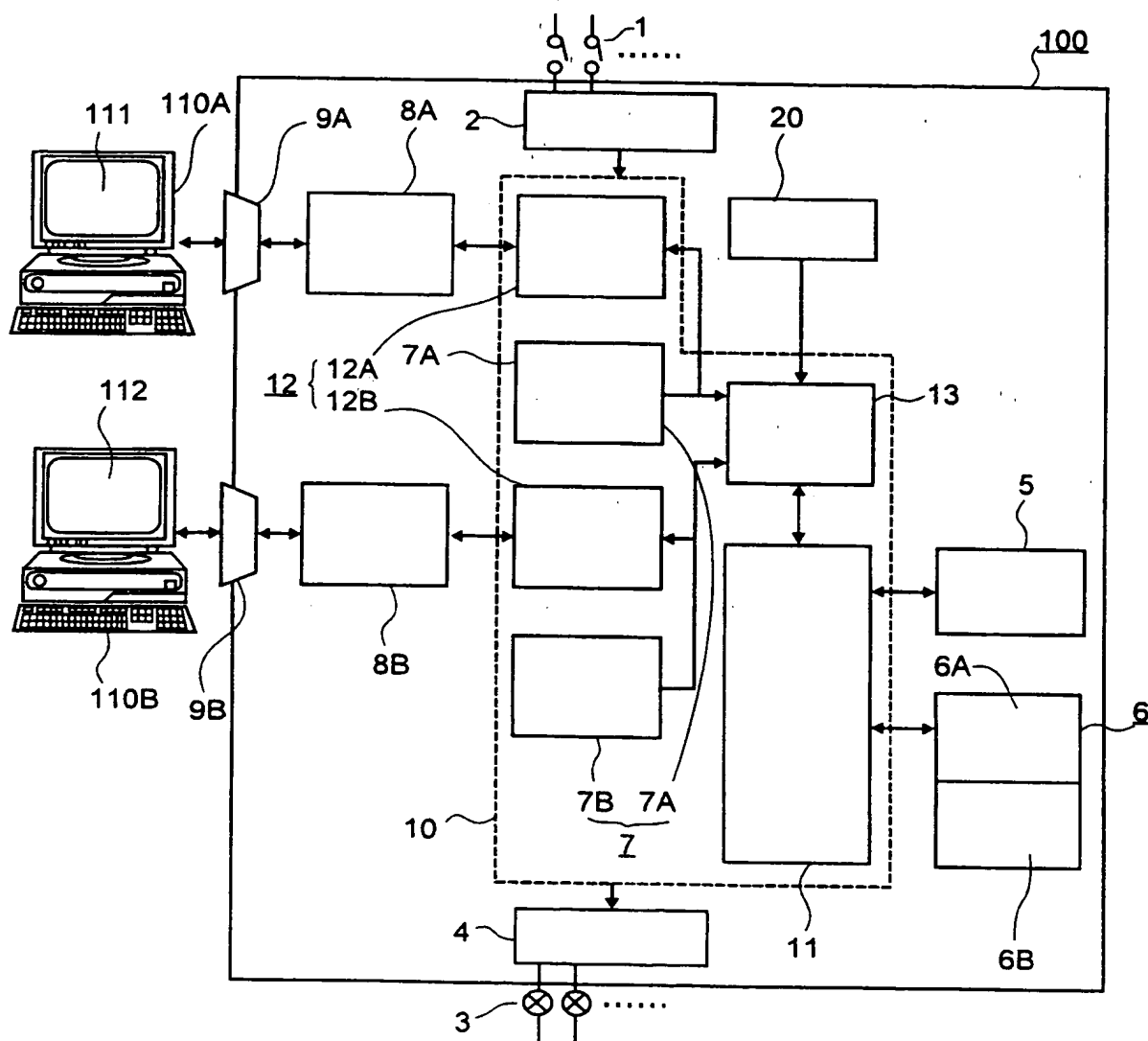


FIG.6

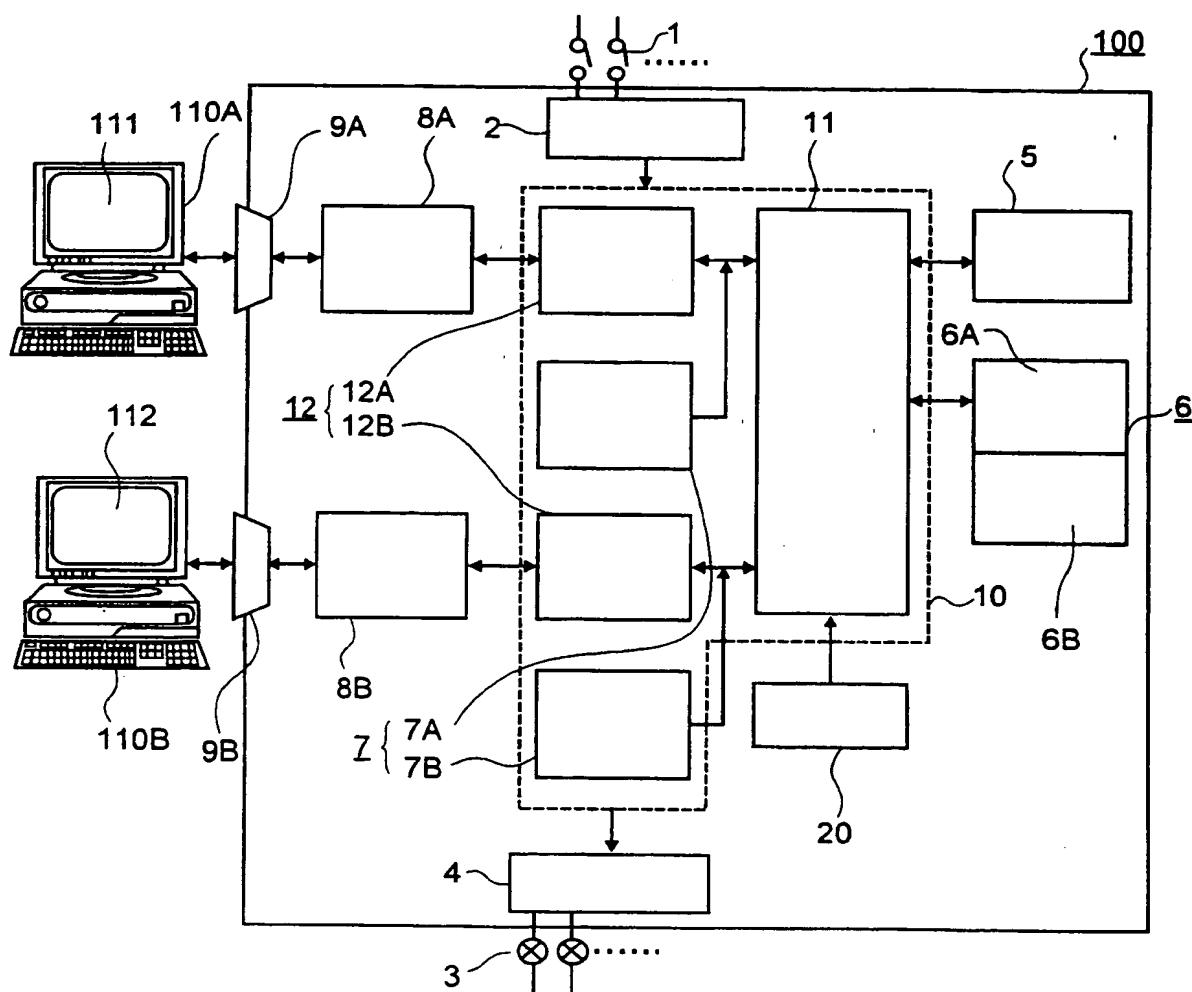


FIG.7

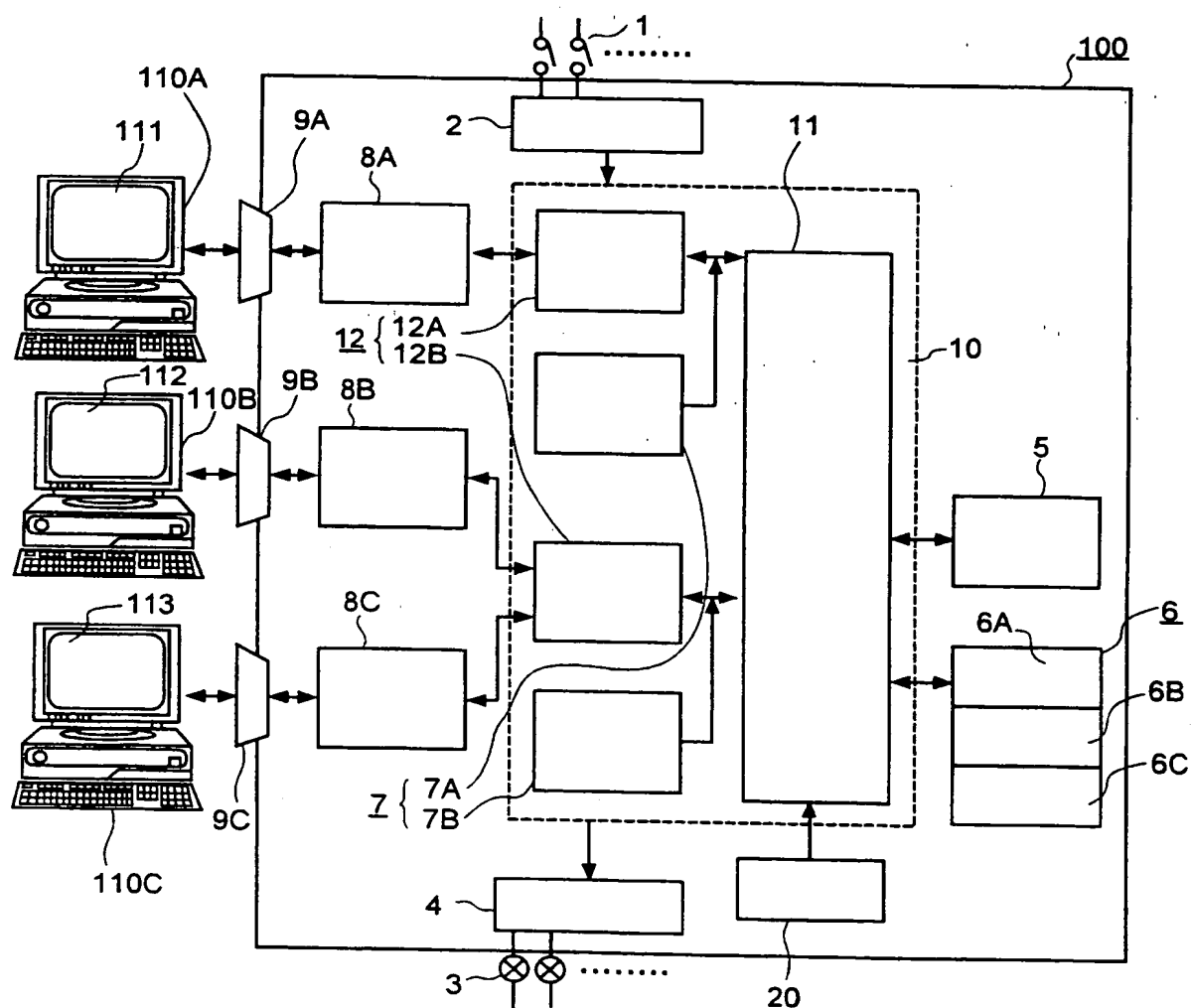
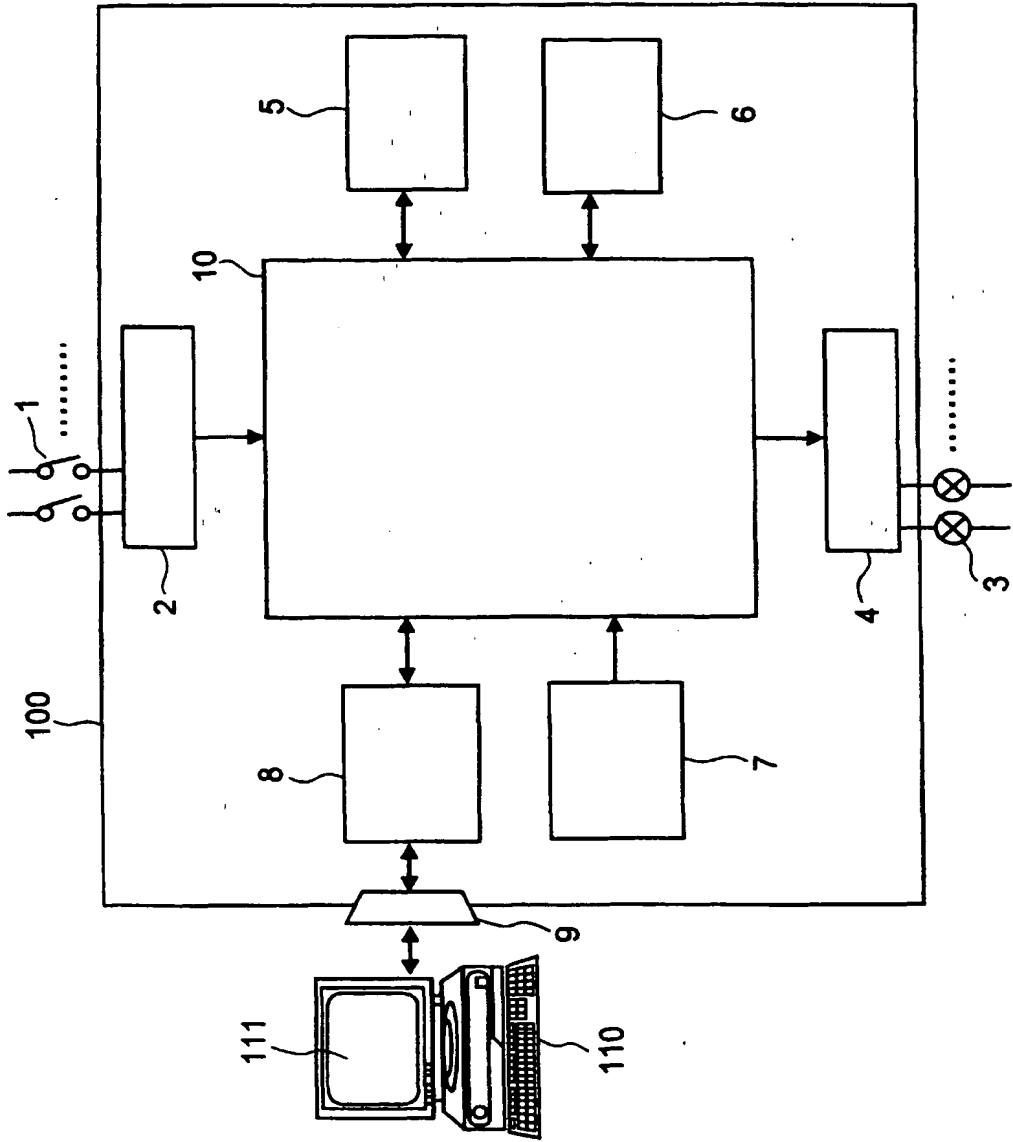


FIG.8



(19)



Europäisches Patentamt

European Patent Office

Office européen des brevets



(11)

EP 0 923 010 A3

(12)

EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
21.08.2002 Bulletin 2002/34

(51) Int Cl.7: G05B 19/042, G05B 19/05

(43) Date of publication A2:
16.06.1999 Bulletin 1999/24

(21) Application number: 98122521.2

(22) Date of filing: 30.11.1998

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU
MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

• Sunaga, Tsutomu, Hitachi Nishi-ryo Room 309,
Kitakanbara-gun, Niigata 959-2604, (JP)
• Seki, Kenji
Toyosaka-shi, Niigata 950-3321 (JP)

(30) Priority: 12.12.1997 JP 34313897

(71) Applicant: Hitachi, Ltd.
Chiyoda-ku, Tokyo 101 (JP)

(74) Representative: Altenburg, Udo, Dipl.-Phys. et al
Patent- und Rechtsanwälte
Bardehle - Pagenberg - Dost - Altenburg -
Geissler - Isenbruck,
Galileiplatz 1
81679 München (DE)

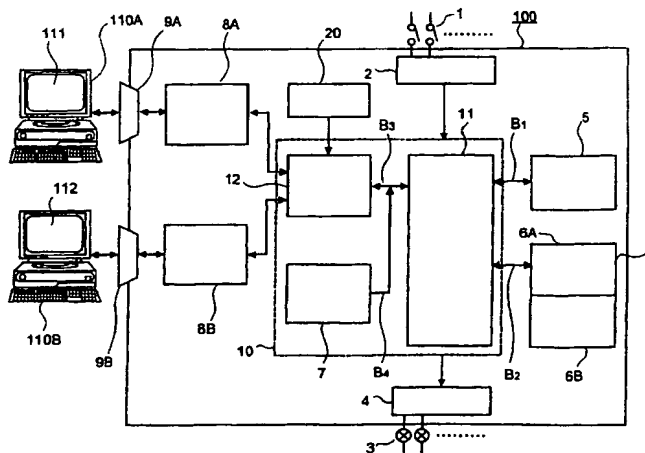
(72) Inventors:
• Kikuchi, Tadanori, Kikuchi Apt. Room 16
Niigata 950-3116 (JP)

(54) Programmable controller

(57) A programmable controller includes a first port 9A for communicating with a first peripheral apparatus 110A, a first interface portion 8A connected with the first port 9A, a second port 9B for communicating with a second peripheral apparatus 110B, a user program memory 6 for storing a user program, a main processor 11 for performing an operation according to the user program, and a sub processor 12 disposed so as to communicate

with the first interface portion 8A, the second interface portion 8B and said main processor 11. The user program memory 6 is divided into at least two memory areas 6A, 6B, and the sub processor 12 controls communication of the first port 9A and the second port 9B with the memory areas 6A, 6B. A programmable controller convenient and efficient in trouble shooting is obtained by this invention.

FIG.1





European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 12 2521

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US 5 212 631 A (SCHMIDT OTOMAR S ET AL) 18 May 1993 (1993-05-18) * column 3, line 56 - column 11, line 5 *	1-3	G05B19/042 G05B19/05
A	EP 0 496 097 A (ALLEN BRADLEY CO) 29 July 1992 (1992-07-29) * column 3, line 51 - column 6, line 17 *	1-3	
A	PATENT ABSTRACTS OF JAPAN vol. 1997, no. 03, 31 March 1997 (1997-03-31) -& JP 08 286712 A (FANUC LTD), 1 November 1996 (1996-11-01) * abstract *	1-3	
A	EP 0 455 345 A (MATSUSHITA ELECTRIC WORKS LTD) 6 November 1991 (1991-11-06) * page 7, line 7 - page 8, line 10; figure 5 *	1-3	
A	DE 34 40 917 A (INTER CONTROL KOEHLER HERMANN) 15 May 1986 (1986-05-15) * page 9, line 24 - page 10, line 29; figure 1 *	1-3	TECHNICAL FIELDS SEARCHED (Int.Cl.6) G05B
The present search report has been drawn up for all claims			
Place of search MUNICH		Date of completion of the search 1 July 2002	Examiner Gardella, S
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

EPO FORM 1503 03.92 (P04C01)

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 98 12 2521

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

01-07-2002

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 5212631	A	18-05-1993	US 5265005 A	23-11-1993
			BR 9103586 A	12-05-1992
			CA 2048944 A1	01-03-1992
			DE 69116954 D1	21-03-1996
			DE 69116954 T2	02-10-1996
			EP 0473086 A1	04-03-1992
			JP 2940841 B2	25-08-1999
			JP 5073112 A	26-03-1993
EP 0496097	A	29-07-1992	BR 9105617 A	01-09-1992
			CA 2056829 A1	27-06-1992
			DE 69124499 D1	13-03-1997
			DE 69124499 T2	21-08-1997
			EP 0496097 A2	29-07-1992
			JP 4303209 A	27-10-1992
			MX 9102710 A1	01-06-1992
JP 08286712	A	01-11-1996	NONE	
EP 0455345	A	06-11-1991	JP 2834837 B2	14-12-1998
			JP 3282904 A	13-12-1991
			DE 69126166 D1	26-06-1997
			DE 69126166 T2	04-12-1997
			EP 0455345 A2	06-11-1991
			KR 9503552 B1	14-04-1995
			US 5371860 A	06-12-1994
DE 3440917	A	15-05-1986	DE 3440917 A1	15-05-1986

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

This Page Blank (uspto)